# Enhanced Damage in Linear Bipolar Integrated Circuits at Low Dose Rate

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## *introduction*

Recent work has shown that total dose effects in some bipolar structures depend on dose rate, exhibiting substantially greater damage under lower dose rate conditions compared to the damage that occurs at high dose rates.[1-5] This poses a major difficulty for space systems, bringing into question much of the archival data on bipolar devices, most of which was taken at high dose rates. Although enhanced damage has been observed for several part types, only a few devices have been investigated in detail because of the cost and time required for low close-rate experiments. A number of issues still need to be addressed, including determination of the underlying mechanisms, establishing variations in the low dose rate response of the same basic part types between different manufacturers, dealing with circuit design issues, and development of practical ways to deal with the problem that can reduce the cost and time required for characterization.

This paper discusses new results for several linear bipolar devices, comparing parts from five different manufacturers. Sensitive device parameters arc determined for several different linear designs, including some devices with more complex input stage designs, ancl two device types with JFET input stages. The JFET devices, for which tests are just beginning, use npn and pnp bipolar devices in subsequent stages

## *Evaluation of Enhanced Damage*

For many linear devices, input bias current can bc used as an approximate measure of the degradation of the internal transistor at the input stage. Recent work has shown that dose rate effects appear to be much larger in the pnp transistor structures which are used i n many commercial bipolar processes than in npn transistors, even for npn devices that are fabricated with the same basic process.[2,5] For some manufacturing processes the damage in pnp devices is 6-7 times greater at low dose rates, and continues to be sensitive to dose rate effects at dose rates as low as 0.005 rad(Si)/s, as shown in Figure 1. Damage in npn devices from similar processes is only about 2.5 times greater at low dose rates, and the npn devices tested to date are no longer dose rate sensitive at dose rates below approximately 1rad(Si)/s. The difference in behavior of npn and pnp damage implies that damage in these two types of transistors will no longer "track" at low dose rates, leading to the possibility of different failure mechanisms under low dose rate conditions. This is an added complication which must be considered in developing alter natives to low dose-rate testing; it may not bc adequate to simply apply a guardband factor to high dose rate results if the failure mechanism is different at low dose rate.

Although evaluating changes in bias current is a useful way to compare the rate at which damage occurs at low and high dose rates, ionization damage is generally nonlinear with dose, and it is necessary to examine circuit performance over a wide dose range in order to accurately determine the effect of dose rate on circuit performance. Figure 2 shows such results for input bias current of an LM111 comparator at SO rad(Si)s and 0.005 rad(Si)/s; the low dose rate tests required six months to complete. The input device is a substrate pnp transistor. Note that under high dose rate conditions the damage saturates at about 100 nA, which is only slightly beyond the. specification limit. At very low dose rates not only is the slope much greater, but the damage saturates at far higher values. For this particular device, the difference in saturation characteristics further magnifies the effect of low dose-rate testing on device failure levels, leading to larger differences than predicted from evaluation of the rate of change of input bias current at low total dose levels. Low dose-rate tests have recently been started for LM 111 comparators from two additional manufacturers, and these results will be presented in the final paper.

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Other circuit parameters are also important. In some cases parameters that exhibit only small changes with dose under high dose-rate conditions can exhibit much larger changes under low dose-rate conditions. This is shown by the results for input offset voltage for the LM324 op-amp in Figure 3. At approximately 25 krad(Si), test results at 0,002 rad(Si)/s exhibit a sudden shift in sign; furthermore, the changes in offset voltage are quite large compared to test results at the same total dose level at higher dose rates. One possible explanation for this behavior is degradation of internal bias circuitry, which causes near catastrophic changes after the threshold for normal operation is exceeded. Figure 4 shows the fractional value of power supply current vs. total dose for these devices. The supply current depends on the gain of internal lateral pnp transistors. Clearly there is a significant difference in the way that the power supply current degrades, even between the two lowest dose rates, 0.002 and 0.005 rad(Si)/s. This suggests that lateral pnp transistors, which have not been directly evaluated for these processes, continue be affected by dose rate even at 0.002 rad(Si)/s.

### *Influence of Circuit Design*

Many linear devices use circuit designs that are far more complicated than the relatively simple designs of the1.M111 and LM 124, Figure 5 shows a simplified schematic of the compensated input stage used in the OP-27 and OP-37 op-amps in which the base current of the npn transistor is partially compensated by current from a lateral-pnp current source. Dose rate effects are far more difficult to evaluate for this type of circuit.

Because of the circuit design, the pnp current source of the OP-27 is only weakly dependent upon pnp transistor gain, so that initially the input bias current will be dominated by gain degradation of the npn device. However, once the pnp gain falls to sufficiently low values, the pnp current source will degrade rapidly, reducing the compensating current and causing a much steeper increase in input current than for an uncompensated input stage. If the pnp devices exhibit more enhanced damage, which was clearly the case for devices from National Semiconductor and Motorola (see Figure 1), then one would expect the failure level of the OP-27 to be much lower at low dose rates, although the dose-rate dependence may not be evident until higher total dose levels.

High and low dose-rate tests of the input bias current of the OP-27 arc shown in Figure 6. Low dose-rate tests are in progress for parts from two vendors, and have reached 17 krad(Si). Although data at higher total dose levels is required to fully determine the effect of low dose rate on the circuit, the initial results show that the increase in current occurs at lower levels at low dose rates, consistent with expectations for this type of design. These tests will be extended to much higher levels during the next few months, and will be included in the full paper, along with results for two device operational amplifiers with JFET input stages, for which circuit design is also a key factor.

### *Stricture and Design of Bipolar Devices*

Work to date on dose rate effects has dealt with three different classes of devices: (1) small-geometry high-speed devices with low voltage ratings (≈ 5 V);[1,4] (2) linear circuits with high breakdown voltage (≈ 40 V) that often usc substrate and lateral pnp transistors in key circuit areas;[2,3,5] and (3) discrete transistors, with a variety of voltage ratings, but much simpler processing.[z] There are significant differences in the way that these devices arc fabricated which have a strong likelihood of affecting the low close-rate response, and make it difficult to reach general conclusions about dose rate effects. The type of device, voltage rating, and isolation technology all affect its susceptibility to ionization damage.

A typical bipolar process involves several oxidation steps. The isolation diffusion step, which is not used for discrete transistors, occurs early in the process. The. oxide thickness that is initially grown must be sufficient to prevent penetration of boron during the isolation diffusion (and subsequent processing steps), except in the regions where it was removed to form the collector isolation region. 'l'his oxide region must be very thick, ≈ 5000-10000 Å, because of requirement to diffuse relatively high boron concentrations through the epitaxial layer, which is typically about 15 µm for linear technologies with high breakdown voltage, but only about 3 µm for lower voltage

devices. The isolation diffusion oxide must be much thicker for high voltage devices; thus, it is likely that ionization damage (and low dose-rate effects) will differ for low- and high-voltage processes.

The thick isolation oxide is selectively removed from different regions during processing. Oxides grown in later steps are much thinner, because they involve relatively shallow diffusions. The isolation oxide is removed prior to the base diffusion, and consequently it is not present over the base or emitter of npn devices. However, it is still present over the collector region, which is the base of substrate and lateral pnp transistors. Thus, the base and emitter-base regions of these pnp transistors have much thicker oxides than npn devices fabricated with the same process. This may be one reason why pnp devices exhibit much more damage at low dose rates, although doping levels and geometry are also contributing factors. [8,9] This will be discussed in more detail in the complete paper.

*Discussion*

At this point there are many unanswered questions about enhanced damage at low dose rates, and no general way to deal with the problem has yet been formulated. The work in this paper will provide additional information about the magnitude of enhanced damage for devices from different manufacturers, as well as additional technologies, including bipolar processes which have been adapted to provide integrated JFET structures.

Very low dose rate tests are clearly impractical for routine evaluation of devices, but are essential in order to provide the technical background for more practical approaches. Preliminary results suggest that there may be large differences in the response of devices from different manufacturing lines at low dose rates, which may provide a possible solution for the low dose-rate problem.

Another important issue is how to apply low dose rate results to real environments. Most space environments do not involve low, constant dose rates, but consist of a very low background dose rate, with occasional short periods of much higher intensity due to passage through radiation belts, or solar flares. This issue will also be addressed in the final paper.

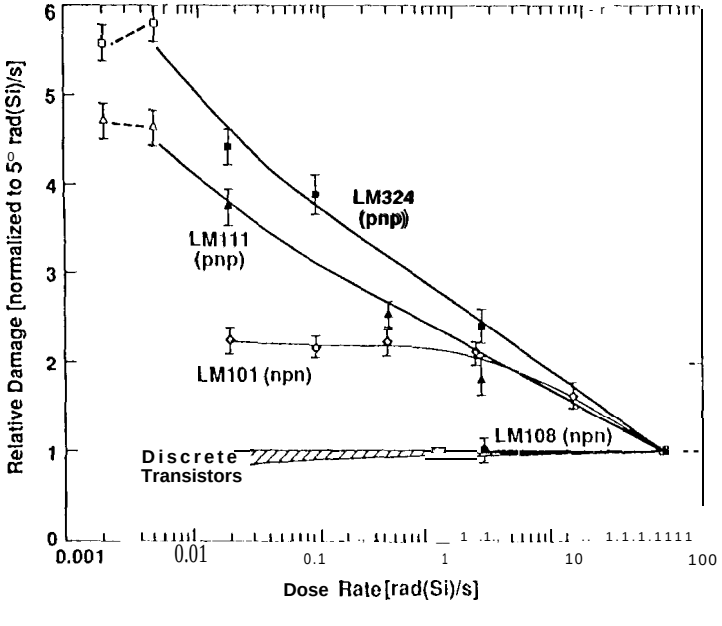


Figure 1. Relative damage vs. dose rate for npn and substrate pnp transistors from linear processes.

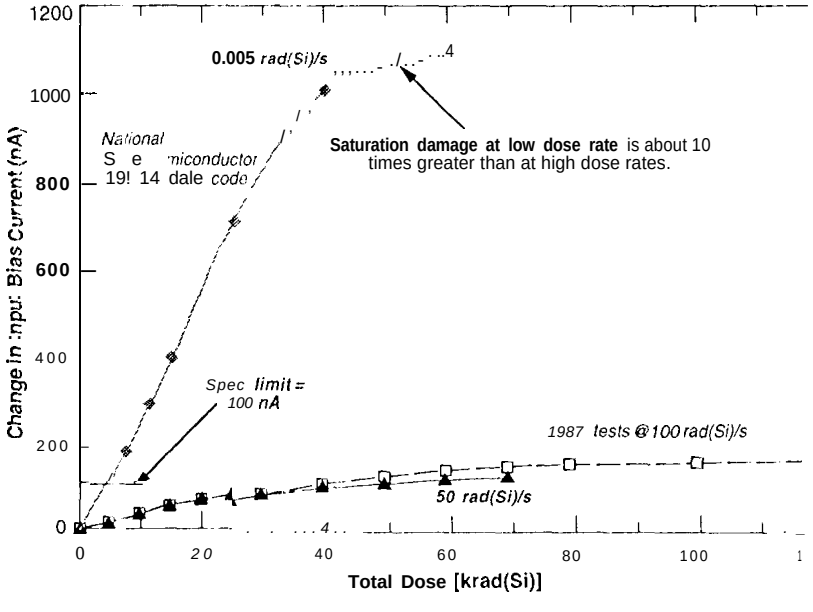


Figure 2. Saturation characteristics of LM111 comparator input current at low and high dose rates.

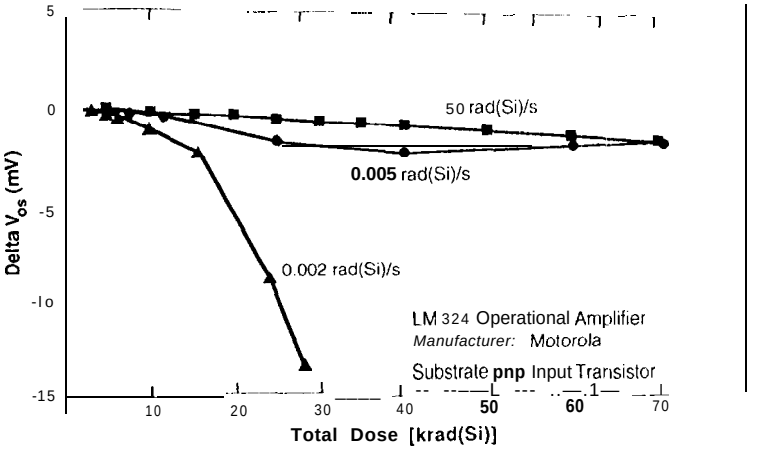


Figure 3. Input offset voltage vs. total dose for the LM324 op-amp at various dose rates.

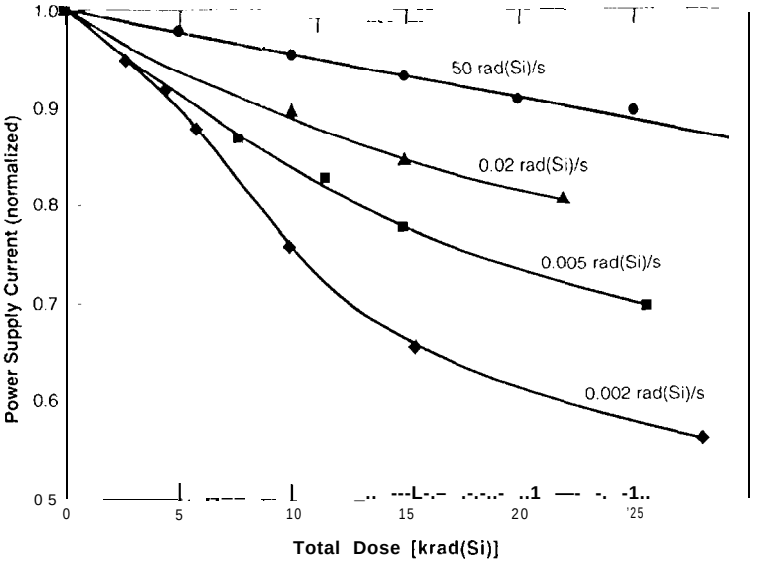


Figure 4. Power supply current vs. total dose for the LM324 op-amp at various dose rates.

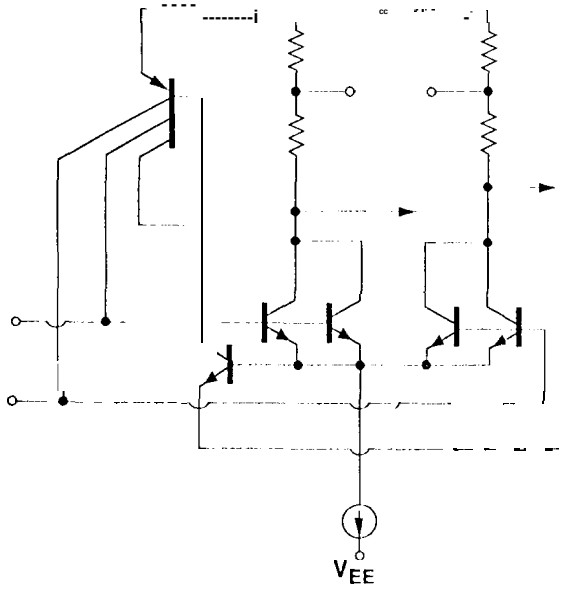


Figure 5. Simplified schematic of the compensated input stage of the OP-27 and OP-37 op-amps.

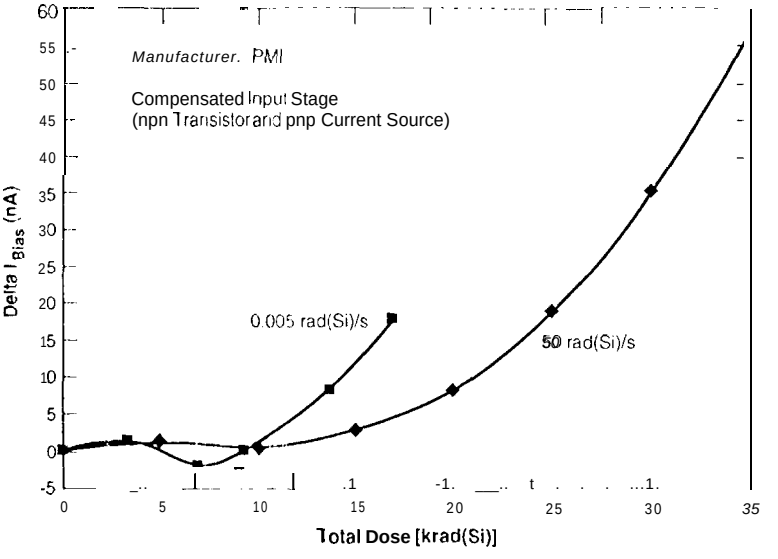


Figure 6. Input bias current vs. total dose for the OP-27 op-amp at high and low dose rates.

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